CLAIMS:

1. A device with a memory, the device comprising
- a matrix of static memory cells functionally arranged in rows and columns;
- bit line circuits, each for writing data to memory cells in a respective one of the columns;
- a word line circuit constructed so that the word line circuit is capable of selecting memory cells in a plurality of the rows simultaneously to receive write data from the bit line driver circuits;
- cell strength control circuitry coupled to the cells and arranged to reduce drive strengths required to write data into individual ones of the memory cells, relative to a drive strength of the bit line circuits, at least during simultaneous writing of data into the memory cells in a plurality of the rows.

2. A device according to Claim 1, wherein the cell strength control circuitry comprises a power supply reduction circuit coupled between a common power supply and an internal power supply line, the memory cells of at least one of the columns having power supply inputs coupled the internal power supply line, the power supply reduction circuit being arranged to provide a power supply voltage drop time-selectively at least during writing of data into the memory cells.

3. A device according to Claim 2, wherein the power supply reduction circuit comprises a resistive element coupled between the common power supply and the internal power supply line.

4. A device according to Claim 2, wherein the resistive element comprises a transistor, with a main current channel coupled between the common power supply and the internal power supply line.

5. A device according to Claim 2, wherein the bit line circuit for the at least one of the columns comprises a bit-line driver circuit with a power supply input coupled to the internal power supply line.

6. A device according to Claim 5, wherein the bit-line driver circuit has a control input coupled to receive a control voltage derived from the common power supply line, substantially unaffected by said drop.

7. A device according to Claim 1, wherein the cell strength control circuitry comprises a plurality of power supply reduction circuits, each coupled between a common power supply and a respective internal power supply line, the memory cells in respective ones of the columns each having power supply inputs coupled a respective one of the internal power supply lines, each power supply reduction circuit being arranged to provide a respective power supply voltage drop on the respective one of the internal power supply lines to which that power supply reduction circuit is coupled, selectively at least during writing of data into the memory cells.

8. A device according to Claim 7, wherein each power supply reduction circuit comprises a resistive element coupled between the common power supply and a respective one of the internal power supply lines.

9. A device according to Claim 7, wherein the bit line circuit for each respective one of the columns comprises a respective bit-line driver circuit with a power supply input coupled to the internal power supply line of that respective one of the columns.

10. A device according to Claim 9, wherein each bit-line driver circuit has a control input coupled to receive a control voltage derived from the common power supply line, substantially unaffected by said drop.